CLAIMS

1. An electronic device formed in a substrate, said device comprising:

a plurality of circuit elements formed in a first surface of said substrate, said plurality of circuit elements including at least one active circuit element and at least one redundant circuit element;

at least one programmable fuse element formed in a second surface of said substrate; said programmable fuse element storing, when said at least one active circuit element is defective, an indication thereof; and

at least one interconnect connecting said plurality of circuit elements and said programmable fuse element.

2. The device of claim 1 further comprising at least one opening formed in said substrate and extending between said first surface and second surface; said interconnect passing through said opening.

3. The device of claim 1 further comprising a plurality of programmable fuse elements formed in said second surface of said substrate.

4. The device of claim 4 wherein said plurality of programmable fuses stores, when said at least one active circuit element is defective, an address thereof.

5. The device of claim 1 wherein said at least one programmable fuse element includes a two-dimensional array of programmable fuse elements and a plurality of leads arranged as rows and columns of a grid, each of said leads being connected to said front surface of said substrate by a respective interconnect, each of said programmable fuse elements providing a respective connection between a particular column lead and a particular row lead.

6. The device of claim 5 wherein values stored in a row of said array of programmable fuse elements are read by sequentially activating each column lead and reading an output on a respective row lead connected to said row of said array of programmable fuse elements.

7. The device of claim 1 wherein said plurality of active circuit elements includes a plurality of memory cells, and said redundant circuit element is a redundant memory cell.

8. An memory device formed in a substrate, said device comprising:

a plurality of circuit elements formed in a first surface of said substrate, said plurality of circuit elements including a plurality of active memory cells and a plurality of redundant memory cells;

a plurality of programmable fuse elements formed in a second surface of said substrate; said programmable fuse elements storing, when said at least one of said plurality of active memory cells is defective, an address thereof; and

a plurality of interconnects connecting said plurality of circuit elements and said programmable fuse elements.

9. The device of claim 8 further comprising a plurality of openings formed in said substrate and extending between said first surface and second surface; a respective one of said plurality of interconnects passing through a respective one of said plurality of openings.

10. The device of claim 8 wherein said plurality of programmable fuse elements is arranged as a two-dimensional array of programmable fuse elements, and said device further comprises a plurality of leads arranged as rows and columns of a grid, each of said leads being connected to said front surface of said substrate by a respective one of said plurality of interconnects, each of said programmable fuse elements providing a respective connection from a particular column lead to a particular row lead.

11. The device of claim 10 wherein values stored in a row of said array of programmable fuse elements are read by sequentially activating each column lead and reading an output on a respective row lead connected to said row of said array of programmable fuse elements.

12. An electronic device formed in a substrate, said device comprising:

a plurality of circuit elements formed in a first surface of said substrate;

at least one bonding pad formed in a second surface of said substrate; and

at least one interconnect connecting said plurality of active circuit elements and said bonding pad.

13. The device of claim 12 further comprising at least one opening formed in said substrate and extending between said first surface and second surface; said interconnect passing through said opening.

14. The device of claim 12 wherein said plurality of circuit elements includes a plurality of memory cells.